

REMARKS

Claims 1-9, 13-17, 20-36 and 39-49 are pending in this application and claims 25-36 are withdrawn from consideration. By this Amendment, claims 1, 4, 8-9, 13-15 and 20-24 are amended, claims 10-12 and 18-19 are canceled, and claims 39-49 are added. Reconsideration based on the above amendments and following remarks is respectfully requested.

I. The Claims Define Patentable Subject Matter

Claims 1-17, 19 and 21-24 are rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,470,787 to Greer in view of U.S. Patent No. 6,441,487 to Elenius et al. This rejection is respectfully traversed.

The applied art does not teach, disclose or even suggest a semiconductor device having insulating layers formed around external terminals on the interconnect pattern, the insulating layers including a first layer and a second layer formed closer to the semiconductor element than the first layer wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer, as claimed in claim 1 and similarly claimed in claims 21 and 23. Further, the applied art does not teach, disclose or suggest the insulating layers including a first layer and a second layer with the second layer formed closer to the semiconductor element than the first layer wherein the Young's modulus of the second layer is greater than the Young's modulus of the first layer, as claimed in claim 39 and similarly claimed in claims 48 and 49.

Instead, Greer discloses a semiconductor device having a semiconductor element 24 and a plurality of electrodes 22. Greer discloses a plurality of passivation layers 26, 28 and 30 formed around the external terminals on the interconnect pattern. Thus, the Office Action asserts that Greer shows a plurality of insulating or passivation layers 26, 28 and 30 formed around the external terminals on the interconnect pattern. The insulating layers include an upper layer 30 and a lower layer of different characteristics (i.e., layer thickness). However,

Greer does not disclose or suggest, nor does the Examiner particularly assert that Greer discloses a first insulating layer and a second layer formed closer to the semiconductor element than the first layer wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer, as claimed in claim 1 and similarly claimed in claims 21 and 23. Nor does Greer disclose that the Young's modulus of the second layer is greater than the Young's modulus of the first layer, as claimed in claim 39 and similarly claimed in claims 48 and 49.

The above recited features and advantages provided by those features are set forth in the specification at least on page 37, lines 3-10 and page 48, lines 1-10, respectively. Specifically, the coefficient of thermal expansion of the lower layer 124 which is closer than the semiconductor chip 110 approaches that of the semiconductor chip and the coefficient of thermal expansion of the upper layer 122 which is closer to the circuit board approaches that of the circuit board. As such, the stress can be effectively absorbed. Additionally, corresponding to the fact that the expansion and contraction of the semiconductor chip 210 is smaller, the first insulating layer 240 which is positioned closer to the semiconductor chip 210 has a larger Young's modulus. The fact that the expansion and contraction of the circuit board is larger, the second insulating layer 242 formed closer to the circuit board has a smaller Young's modulus. Accordingly, with the first and second insulating layers 240 and 242 having different characteristics, the stress can be effectively absorbed.

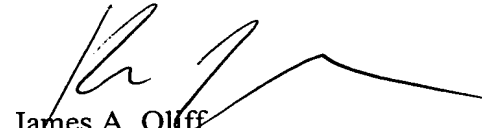
None of the applied art teaches, discloses or even suggests the features recited in the independent claims discussed above. Accordingly, the applied art does not provide at least the advantages discussed above. Withdrawal of the objection of the claims under 35 U.S.C. §103(a) as unpatentable over Greer in view of Elenius is respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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